case, each sync block 103 generates, from each incoming received signal sample stream, two samples per symbol period (that is, M=2), corresponding to two different sample phases. Thus, in FIG. 1, samples r.sub.a,0 (n) and r.sub.a,1 (n), where n is the time index, are generated from the signal sample stream received by an antenna a. Similarly, samples r.sub.b,0 (n), r.sub.b,1 (n) and r.sub.c,0 (n), r.sub.c,1 (n) are generated from the two sample streams received from the other two antennas b and c respectively. The samples from the sync blocks 103 are passed to a branch metric pre-processor 104, which also receives channel tap estimates from respective channel tap estimators 105, of which there is one for each of the signals r.sub.a (n)-r.sub.c (n).

The branch metric pre-processor 104 also receives an input from an impairment correlation estimator 106, which estimates the impairment correlation properties over the antennas and sampling phases, as will be described in more detail below.

In the illustrated embodiment, the branch metric pre-processor calculates metric multipliers e(j,n), f(j,n) and g(j,k,n), which are used by the branch metric processor 107 to compute the branch metric M.sub.h (n), which is passed to the sequence estimation processor 108 to determine the estimated symbol sequence S. The calculation of the metric multipliers and the computation of the branch metric is described in more detail on pages 18-19 of WO96/04738.

As mentioned previously, the processing unit 102 as described so far is known, for example from the document WO96/04738 mentioned above.